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| EXAMINER | |
|---|---|
| GERSTL, SHANE F | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/917,312 | CHENG ET AL. | |
| | Examiner | Art Unit | |
| | Shane F Gerstl | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-13 have been examined.

### *Papers Received*

2. Receipt is acknowledged of the amendment papers submitted, where the papers have been placed of record in the file.

3. The amendment has successfully overcome the objections to the title and claims, which are herein withdrawn. The duplicate claim issue indicated in the previous Action also no longer exists by virtue of the current amendment.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-10, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Parady (5,933,627).

6. In regard to claim 1, Parady discloses a processing system (figure 3) for processing information efficiently and cost-effectively by switching between execution of time-critical and non-time-critical tasks comprising:

a. a processing unit (figure 1, element 41)

b. a first register group coupled to said processing unit and including a first set of registers (figure 3, element 48, thread 0), said first register group designated only for updating the status of said first set of registers,

said processing unit reading the status of said first set of registers to execute only time-critical tasks; [The examiner is interpreting the term "status" according to the including IEEE dictionary definition, which states, "the condition at a particular time of a system or system component." Thus the status of a set of registers (system components) may be viewed as the data within those registers, which is a condition at that particular time until overwritten. Figure 3 shows that each thread has it's own separate register file (element 48), which is a group of registers including some first set of registers, which may be any subset of the file or the entire file, and thus the group or register file only updates the registers within it. Figure 3 shows that the execution units or processing unit read the data (shown above to be the status) from the registers. Column 4, lines 22-24 show that in one embodiment a priority thread is provided with transitions from other threads always going back to the priority thread and thus the priority thread is a time-critical thread since it is always executed when possible. Therefore, the registers dedicated to the priority or time-critical thread are used only to execute tasks or instructions from the time-critical or priority thread.]

c. and a second register group coupled to said processing unit and including a second set of registers (figure 3, element 48, thread 1), said second register group designated only for updating the status of said second set of registers, said processing unit reading the status of said second set of registers to execute non-time-critical tasks, said processing

unit switching to execute only non-time-critical tasks by avoiding saving the status of said first set of registers; [As shown above, each thread has it's own register file and all instructions or tasks other than the priority or time-critical tasks are non-time-critical tasks since they are only processed when the priority thread cannot process. Thus, every other thread executes non-time-critical tasks. The status of the first set of registers has no need to be saved since they will not be overwritten by other threads in the processor.]

d. wherein said processing unit switches between executing time-critical tasks and non-time-critical tasks efficiently and cost-effectively by avoiding saving status of the first or second set of registers. [As shown above there is no need in Parady to save the status of the registers on a context switch between the time-critical and non-time-critical tasks because each thread has its own set of dedicated registers.]

7. In regard to claim 2, Parady discloses a processing system as recited in claim 1 wherein said processing unit switches to executing said time-critical tasks by avoiding saving the status of said second set of registers (as shown above).

8. In regard to claim 3, Parady discloses a processing system as recited in claim 1 further including a code random access memory (RAM) for storing instructions wherein said code RAM is designated only for execution of said time-critical tasks, said processing unit fetching instructions from said code RAM to execute said time-critical tasks. [Figure 3 shows that each thread has its own instruction (or code) buffer and thus there is a separate buffer for the time-critical

thread. The included dictionary definition of RAM provides for a computer memory, the contents of which can be altered at any time. Clearly a buffer can be accessed and altered at any time and thus is a code RAM.]

9. In regard to claim 4, Parady discloses a processing system as recited in claim 1 further including an instruction cache (I-cache) for storing instructions wherein said instruction cache is designated only for execution of said non-time-critical tasks, said processing unit fetching instructions from said instruction cache to execute said non-time-critical tasks. [Figure 3 shows that each thread has its own instruction buffer and thus there is a separate buffer for each non-time-critical thread. The included dictionary definition of cache provides for a high speed buffer storage that is continually updated to contain recently accessed contents of main storage. The buffers of figure 3 are continually updated to contain instructions fetched from the main on-chip storage (the higher level instruction cache of figure 1, which is inherently addressed) and thus are caches in themselves.]

10. In regard to claim 5, Parady discloses a processing system as recited in claim 1 further including a first data memory designated only for storing data for executing said time-critical tasks, said processing system further including a second data memory designated only for storing data for executing said non-time-critical tasks. [The registers files discussed previously for each thread are in themselves data memories and hold data for execution of either only time-critical or only non-time-critical tasks depending on the associated thread.]

11. In regard to claim 6, Parady discloses a processing system as recited in claim 5 further including a data bus bridge for transferring data from an external memory to said second data memory. [Figure 1 (which is shown to be the base processor for the invention in column 2, lines 66-67) shows that the data memories (registers) have a data bridge (cache control, element 22) for transferring data from an external memory (figure 2).]

12. In regard to claim 7, Parady discloses a processing system as recited in claim 1 further including a low priority interrupt controller responsive to interrupt commands requesting service, said low priority interrupt controller signaling said processing unit to provide service by executing said non-time-critical tasks. [As shown in the abstract, context switches occur on long-latency events. Thus when the priority (high priority) thread introduced earlier is executing and encounters a long-latency event, an interrupt is issued to switch to a lower priority thread, which executes non-time-critical tasks. There is inherently a controller for this interrupt, which may be appropriately named a low priority interrupt controller since an interrupt is issued to switch to a lower priority thread.]

13. In regard to claim 8, Parady discloses a processing system as recited in claim 1 further including a high priority interrupt controller responsive to interrupt commands requesting service, said high priority interrupt controller signaling said processing unit to provide service by executing said time-critical tasks. [As shown above, the priority thread is always switched back to from other threads. This is most likely done on a long-latency event such as described in the

abstract, which causes an interrupt and a switch back to the priority thread. There is inherently a controller for this interrupt.]

14. In regard to claim 9, Parady discloses a processing system as recited in claim 1 wherein said processing system is in communication with a communication system, said processing system further including a register bus (R-bus) bridge for providing an interface between said processing system and said communication system. [Figure 1 (which is shown to be the base processor for the invention in column 2, lines 66-67) shows that the data memories (registers) have a register bus bridge (cache control/system interface, element 22) for providing an interface and transferring data from an external memory (figure 2) to the registers. Since the processing system and the external cache system communicate with each other they are both communication systems and thus the processing system communicates with a communication system.]

15. In regard to claim 10, Parady discloses a processing system as recited in claim 1 further including a real-time operating system (RTOS) for providing services for execution of said non-time-critical tasks. [Column 4, lines 32-41 show an embodiment where the processing system is used for an operating system. The enclosed IEEE standard definition of "operating system" states that an operating system controls execution of a computer program. This means that the operating system given by Parady controls the execution of (or provides services for) all program instructions including non-time-critical tasks. The included IEEE standard definition of "real time system" shows that this is a system where both the computational result and the time at which they are

computed and output are important. The pipelined superscalar processor of Parady is inherently dependent on computational output time so that instructions are properly scheduled for execution and thus the operating system is inherently a real-time operating system that controls this execution.]

16. In regard to claim 13, Paraday discloses a method for processing information efficiently and cost-effectively by switching between execution of time-critical tasks and non-time-critical tasks comprising:

a. updating the status of a first set of registers within a first register group; [Figure 3, element 48 shows a first group of registers for thread 0 that are updated by the results from the execution units.]

b. reading the status of the first set of registers to execute only time critical tasks; [Figure 3 shows that the execution units read the status of the registers as well. Column 4, lines 22-24 show that in one embodiment a priority thread is provided with transitions from other threads always going back to the priority thread and thus the priority thread is a time-critical thread since it is always executed when possible. Therefore, the registers dedicated to the priority or time-critical thread are used (and the data therein read) only to execute tasks or instructions from the time-critical or priority thread.]

c. updating the status of a second set of registers within a second register group; [Figure 3, element 48 shows a second group of registers for thread 1 that are updated by the results from the execution units.]

d. reading the status of the second set of registers to execute only non-time-critical tasks, [Figure 3 shows that the execution units read the status of the registers. As shown above, each thread has it's own register file and all instructions or tasks other than the priority or time-critical tasks are non-time-critical tasks since they are only processed when the priority thread cannot process. Thus, every other thread executes non-time-critical tasks.]

e. and switching to execute non-time-critical tasks by avoiding saving the status of the first set of registers. [There is no need in Parady to save the status of the registers on a context switch between the time-critical and non-time-critical tasks because each thread has its own set of dedicated registers which will not be overwritten.]

***Claim Rejections - 35 USC § 103***

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady in view of Kiriyama (5,561,466).

19. In regard to claim 11,

a. Parady discloses a processing system as recited in claim 1. Parady has shown in column 2, lines 66-67 that the invention is

implemented on an UltraSparc microprocessor. The included Tremblay reference is a document on the structure of the UltraSparc processor and shows in section VII, which starts on page 1661, that there is multimedia support and thus support for video and audio and thus the disclosure of Parady inherently has support for audio and video processing.

b. Parady does not explicitly disclose wherein said processing system is employed in an audio and video encoder/decoder (codec), said audio and video codec performing compression of audio data and video data to generate a compressed audio stream and a compressed video stream.

c. Kiriyama has disclosed an audio/video multiplexer and demultiplexer system (title) that encodes video and audio (figure 5, elements 37 and 45) as well as decodes video and audio (figure 8, elements 73 and 79). Column 4, lines 37-43 show that the video encoding uses data compression in an embodiment. Column 4, lines 60-64 show that the audio data is digitized in the same manner as the video and thus in an embodiment can also be compressed.

d. Column 1, line 63 – column 2, line 5 show that the invention of Kiriyama achieves excellent efficiency and allows reproduction of synchronous audio and video data so that there is no audio-visual gap in this data. This efficiency and audio/video synchronization would have motivated one of ordinary skill in the art to modify the design of Parady to manipulate audio and video data and tasks as taught by Kiriyama.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Parady to manipulate audio and video data and tasks as taught by Kiriyama so that excellent efficiency and synchronous audio and video data may be realized.

20. In regard to claim 12,

a. Parady discloses a processing system as recited in claim 1. Parady has shown in column 2, lines 66-67 that the invention is implemented on an UltraSparc microprocessor. The included Tremblay reference is a document on the structure of the UltraSparc processor and shows in section VII, which starts on page 1661, that there is multimedia support and thus support for video and audio and thus the disclosure of Parady inherently has support for audio and video processing.

b. Parady does not explicitly disclose wherein said non-time-critical tasks include multiplexing of said compressed audio stream with said compressed video stream, said time-critical tasks including providing video data for compression thereof.

c. Kiriyama has disclosed an audio/video multiplexer and demultiplexer system (title) that encodes video and audio (figure 5, elements 37 and 45) as well as decodes video and audio (figure 8, elements 73 and 79). Column 4, lines 37-43 show that the video encoding uses data compression in an embodiment. Column 4, lines 60-64 show that the audio data is digitized in the same manner as the video and thus in an embodiment can also be compressed. This compressed audio and

video data is then multiplexed as shown in figure 5 with element 43. It is well known to one of ordinary skill in the art that the function of multiplexing generally takes less time than the encoding and compressing step that is being done by Kiriyama. Thus the multiplexing function fits the above usage of non-time-critical task and the compression/encoding function fits the usage of time-critical task since it is a longer-latency event.

d. Column 1, line 63 – column 2, line 5 show that the invention of Kiriyama achieves excellent efficiency and allows reproduction of synchronous audio and video data so there is no audio-visual gap in this data. This efficiency and audio/video synchronization would have motivated one of ordinary skill in the art to modify the design of Parady to manipulate audio and video data and tasks as taught by Kiriyama.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Parady to manipulate audio and video data and tasks as taught by Kiriyama so that excellent efficiency and synchronous audio and video data may be realized.

***Response to Arguments***

21. Applicant's arguments filed 8/20/04 have been fully considered but they are not persuasive.

22. Applicant has argued that Parady does not in way teach or disclose "the designation only of a first register group for updating the status of a first set of registers" and similarly for a second group and set of registers. The Examiner is

interpreting the term "status" according to the including IEEE dictionary definition, which states, "the condition at a particular time of a system or system component." Thus the status of a set of registers (system components) may be viewed as the data within those registers, which is a condition at that particular time until overwritten. Figure 3 shows that each thread has it's own separate register file (element 48), which is a group of registers including some first set of registers, which may be any subset of the file or the entire file, and thus the group or register file only updates the registers (and status therein) within it.

23. Applicant further argues that the reference does not teach "the reading of the status of the first set of registers is to execute only time-critical tasks" and similarly for non-time-critical tasks with the second set of registers. Figure 3 shows that the execution units or processing unit read the data (shown above to be the status) from the registers. Column 4, lines 22-24 show that in one embodiment a priority thread is provided with transitions from other threads always going back to the priority thread and thus the priority thread is a time-critical thread since it is always executed when possible. Therefore, the registers dedicated to the priority or time-critical thread are used only to execute tasks or instructions from the time-critical or priority thread and likewise the registers dedicated to the other threads are for non-time-critical tasks.

24. Applicant then argues that Parady does not teach the designation only of particular processing resources for executing either time-critical or non-time-critical tasks only. As shown directly above, Parady does disclose designation of particular register files for certain threads, one of which being time-critical and the

others non-time critical. Further, figure 3 shows that each thread has its own instruction (or code) buffer and thus there is a separate buffer for the time-critical thread. The included dictionary definition of RAM provides for a computer memory, the contents of which can be altered at any time. Clearly a buffer can be accessed and altered at any time and thus is a code RAM. Also, figure 3 shows that each thread has its own instruction buffer and thus there is a separate buffer for each non-time-critical thread. The included dictionary definition of cache provides for a high speed buffer storage that is continually updated to contain recently accessed contents of main storage. The buffers of figure 3 are continually updated to contain instructions fetched from the main on-chip storage (the higher level instruction cache of figure 1, which is inherently addressed) and thus are caches in themselves. Finally, the registers files discussed previously for each thread are in themselves data memories and hold data for execution of either only time-critical or only non-time-critical tasks depending on the associated thread.

25. Applicant's arguments regarding claims 11 and 12 fail to fully comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. It is noted that Applicant believes claims 11 and 12 to be patentable due to their dependence on claim 1, which has been previously argued, however it seems Applicant is attempting to argue the individual limitations of claims 11 and 12 by saying, "Also, the Parady reference, the Kiriyama reference, and/or the combination

thereof do not teach or suggest claims 11 and 12." However, this simple statement does not suffice as pointing out how the particular language of claims 11 and 12 is patentably distinguishable.

***Conclusion***

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

27. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is

(571) 272-4166. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
February 2, 2005

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